

ABSTRACT OF THE DISCLOSURE

A chain type ferroelectric random access memory has a memory cell unit including ferroelectric memory cells electrically connected in series to each other, a plate line connected to an electrode of the memory cell unit, a bit line connected to the other electrode of the memory cell unit via a switching transistor, a sense amplifier which amplifies the voltages of this bit line and its complementary bit line, and a transistor inserted between the switching transistor and the sense amplifier. A value, being the minimum value of the gate voltage in the transistor obtained during elevation of the plate line voltage and comparative amplification, is smaller than a value, being the maximum value of the gate voltage in the transistor obtained during fall of the plate line voltage and comparative amplification. With these features, decrease in the accumulated charge of polarization in the memory cell is reduced and occurrence of disturb is prevented during read/write operations.